REMARKS

Claims 1-24 are pending in this application. The Examiner rejected Claims 1-24. The foregoing amendments and the following comments are responsive to the rejections set forth by the Examiner in the January 5, 2006 Office Action. Reconsideration of the application, as amended, is respectfully requested.

I. SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT & NOTICE OF COPENDING APPLICATIONS

Applicant hereby submits a Supplemental Information Disclosure Statement & Notice of Copending Application. The Supplemental Information Disclosure Statement cites references from the copending application. While the Applicant does not believe that these references will affect the patentability of the pending claims, Applicant respectfully requests the Examiner to consider the pending claims in connection with these references in order to make them of record.

II. REJECTION OF CLAIMS 1-10 AND 12-24 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-10 and 12-24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,157,182 issued to Tanaka, et al. ("the Tanaka patent") in view of U.S. Patent No. 6,229,293 issued to Farrenkof ("the Farrenkof patent") and U.S. Patent No. 6,204,650 issued to Shimamori ("the Shimamori patent"). According to the Examiner, the combined references teach a dual-mode (Fig. 9 of the Tanaka patent) pulse frequency modulation (Fig. 19 of the Shimamori patent) boost converter (Fig. 1 of the Farrenkof patent). In view of the above claim amendments and the following discussion, Applicant respectfully traverses this rejection.

A. Claim 1

Focusing in particular on Claim 1 and the embodiment shown in Figures 2A and 2B, a dual-mode pulse frequency modulation boost converter comprises a power conversion circuit that receives an input voltage (VS) 102 at a first level and that generates an output voltage at a second level. The power conversion circuit includes a switching transistor 106 to generate the output voltage. A pulse frequency modulator 108 is configured to control the switching transistor 106.

An inner control loop 200 senses a switching current (I-SENSE) flowing through the switching transistor 106 and generates a first feedback signal to the pulse frequency modulator 108 to turn the switching transistor 106 off for a predefined duration when the switching current (I-SENSE) reaches a predetermined level (I-REF). The predetermined level (I-REF) is substantially constant (HYST-LEVEL) in a first mode and is controlled by an output voltage feedback signal (CSM-LEVEL) in a second mode. An output control loop 202 senses a load current (V-FB) and turns the pulse frequency modulator 108 off when the load current (V-FB) is greater than a reference level (V-REF) during the first mode. The output control loop 202 forces the pulse frequency modulator 108 to stay on during the second mode.

The Tanaka patent appears to teach a dual-mode converter that uses two sets of control circuits to drive a switch. Referring to Fig. 9 of the Tanaka patent, a switch 21 is coupled to an input voltage (Vin) and selectively turns on/off to generate an output voltage (Vout) connected to a load. For light load currents, the switch 21 is controlled by a light load mode controlling circuit comprising comparators 25, 26 that sense a charging current (I_L) and a comparator 22 that senses the output voltage (Vout). For heavy load currents, the switch 21 is controlled by a PWM controlling circuit 45 that senses the output voltage (Vout). Control signals at respective outputs of the light load mode controlling circuit and the PWM controlling circuit 45 are provided to selectors 43, 44. A mode switching controlling circuit 49 determines whether the converter is operating under light load currents or heavy load currents and controls the selectors 43, 44 to pass the appropriate control signals to drive the switch 21.

The Examiner asserts that Claim 1 of the present invention is taught by replacing the PWM controlling circuit 45 of the Tanaka patent with a PFM controller from the Shimamori patent and adapting the PFM controller for boost converter operation as discussed in the Farrenkopf patent. The Applicant respectfully disagrees with the Examiner's assertion.

First, there is no motivation to replace the PWM controlling circuit 45 of the Tanaka patent with a PFM controller. The Tanaka patent discloses using the light load mode controlling circuit and the PWM controlling circuit 45 to operate a converter in two modes to overcome deficiencies of a PFM system described in its background section. Thus, the Tanaka patent teaches away from replacing the PWM controlling circuit 45 with a PFM controller.

Second, the combination suggested by the Examiner does not teach Claim 1. Assuming that the PWM controlling circuit 45 is replaced with a PFM controller, the combination teaches a modified dual-mode converter that selects between the light load mode controlling circuit and the PFM controller to drive the switch 21 under different load current conditions. That is, the light load mode controlling circuit is used to control the switch 21 during light load currents while the PFM controller is used to control the switch 21 during heavy load currents. The combination does not teach a dual-mode converter with a pulse frequency modulator having control loops that operate in two modes.

Because the references cited by the Examiner do not disclose, teach or suggest a pulse frequency modulator with an inner control loop and an outer control loop having a first mode and a second mode, Applicant asserts that Claim 1 is not obvious in view of the Tanaka patent, the Farrenkopf patent and the Shimamori patent. Applicant therefore respectfully submits that Claim 1 is patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claim 1.

B. Claim 2

Claim 2 is directed to a dual-mode switching regulator comprising a switch and a pulse frequency modulator that controls switching cycles of the switch. The dual-mode switching regulator further comprises a first feedback loop that detects when the switch conducts a current above a selected threshold during each switching cycle and outputs a peak-current detection signal to the pulse frequency modulator in response to turn off the switch for a predefined duration. The selected threshold is a substantially fixed threshold in a first mode and a variable threshold in a second mode.

The references cited by the Examiner do not disclose, teach or suggest a first feedback loop for a pulse frequency modulator that uses a substantially fixed threshold in a first mode and a variable threshold in a second mode to monitor current conducted by a switch. Accordingly, Applicant submits that Claim 2 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 2.

C. Claims 3-10

Claims 3-10, which depend from Claim 2, are believed to be patentable for the same reasons articulated above with respect to Claim 2, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 3-10.

D. Claim 12

Claim 12 is directed to a switching converter that comprises a semiconductor switch and a pulse frequency modulation controller configured to turn the semiconductor switch on and off. The switching converter also comprises a peak current detector configured to sense current flowing through the semiconductor switch and to output a peak current pulse to the pulse frequency modulation controller when the sensed current is above a reference peak level. The pulse frequency modulation controller turns off the semiconductor switch for a predetermined duration in response to the peak current pulse.

The switching converter further comprises a feedback voltage detector and a load sensor. The feedback voltage detector is configured to sense an output voltage of the switching converter and to output a control signal to the pulse frequency modulation controller. The control signal is in an active phase to turn on the pulse frequency modulation controller when the sensed output voltage is less than a first predefined voltage and is in an inactive phase to turn off the pulse frequency modulation controller when the sensed output voltage is greater than a second predefined voltage. The load sensor is configured to detect load current and to output an override control signal to force the pulse frequency modulation controller to remain on when the load current is greater than a predetermined level. The reference peak level of the peak current detector is a variable peak level that varies with the sensed output voltage when the override control signal is active.

The references cited by the Examiner do not disclose, teach or suggest a peak current detector for a pulse frequency modulation controller that uses a variable reference peak level when the load current is greater than a predetermined level (i.e., when the override control signal is active and forces the pulse frequency modulation controller to remain on regardless of the control signal from the feedback voltage detector). Applicant therefore respectfully submits that

Claim 12 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 12.

E. Claims 13-18

Claims 13-18, which depend from Claim 12, are believed to be patentable for the same reasons articulated above with respect to Claim 12, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 13-18.

F. Claim 19

Claim 19 is directed to a method for improving efficiency of a switching regulator that uses pulse frequency modulation to control a switch. The method comprises turning on a pulse frequency modulator for a burst period when an output of the switching regulator is less than a first level. One or more switching cycles for the switch occur in the burst period. The method also comprises turning on the switch in each switching cycle until the switch conducts a peak current followed by a switch off-time of a predetermined duration. The method further comprises operating the switching regulator in a hysteretic mode for a first range of load currents and in a continuous mode for a second range of load currents. In the hysteretic mode, the peak current for the switch is substantially fixed and the pulse frequency modulator turns off when the output of the switching regulator is greater than a second level. In the continuous mode, the peak current for the switch varies according to a feedback signal indicative of an output of the switching regulator and the pulse frequency modulator is forced on to extend the burst period until the variable peak current is less than a predefined level.

The references cited by the Examiner do not disclose, teach or suggest a pulse frequency modulator that controls a switch using a substantially fixed peak current in a hysteretic mode and a variable peak current in a continuous mode. Accordingly, Applicant submits that Claim 19 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 19.

G. Claims 20-22

Claims 20-22, which depend from Claim 19, are believed to be patentable for the same reasons articulated above with respect to Claim 19, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 20-22.

H. Claim 23

Claim 23 is directed to a switching regulator using a dual-mode pulse frequency modulation technique. The switching regulator comprises means for operating in a hysteretic mode and means for operating in a continuous mode. Regulation of an output of the switching regulator is performed using a pulse frequency modulator to operate a switch with a substantially fixed peak switching current in the hysteretic mode and a variable peak switching current in the continuous mode.

The references cited by the Examiner do not disclose, teach or suggest a pulse frequency modulator that operates a switch with a substantially fixed peak switching current in a hysteretic mode and a variable peak switching current in a continuous mode. Accordingly, Applicant submits that Claim 23 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 23.

I. Claim 24

Claim 24, which depends from Claim 23, is believed to be patentable for the same reasons articulated above with respect to Claim 23, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claim 24.

III. REJECTION OF CLAIM 11 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claim 11 as obvious in light of the Tanaka patent and U.S. Patent No. 6,791,283 to Bowman, et al. ("the Bowman patent"). Claim 11, which depends from Claim 2, is believed to be patentable for the same reasons articulated above with respect to Claim 2, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claim 11.

IV. CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain to be resolved, the Examiner is cordially invited to contact the undersigned such that any remaining issues may be promptly resolved. Also, please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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